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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 200205662-1

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on 03/14/2006

Signature: Colleen F. Brown

Typed or printed name: Colleen F. Brown

Application Number	Filed
10/695,363	10/28/2003

First Named Inventor: Stewart R. WYATT

Art Unit	Examiner
2182	Scott C. Sun

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number 54,036
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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03/14/2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [x] *Total of one (1) forms are submitted.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Stewart R. WYATT et al.	§	Confirmation No.:	5968
Serial No.:	10/695,363	§	Group Art Unit:	2182
Filed:	10/28/2003	§	Examiner:	Scott C. Sun
For:	A System Having A Storage Controller That Modifies Operation Of A Storage System Based On The Status Of A Data Transfer	§	Docket No.:	200205662-1

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: March 14, 2006

Sir:

Appellants hereby submit this Pre-Appeal Brief Request for Review in connection with the above-identified application. A Notice of Appeal is filed concurrently herewith. This Brief addresses the rejection of claims 1-2 and 4-9.

Claim 1, in part, requires "to conserve power, the storage controller modifies operation of the storage system based on a status of the data transfer." Claim 1 further requires that "the storage controller modifies operation of the storage system by turning off a portion of the storage system."

The Examiner recognizes that Trost does not disclose "the storage controller modifies operation of the storage system by turning off a portion of the storage system" as required in claim 1, but asserts that White's sleep mode results in turning off an error correction decoding circuit 5. White does not explicitly teach the error correction decoding circuit 5 is turned off during the sleep mode. Instead, White teaches the error correction decoding circuit 5 receives a sleep on/sleep off signal and initiates decoding when re-entering a normal mode (paragraph [0020]). The sleep ON/sleep OFF signal does not necessarily relate

to an on/off state. For example, White's refresh period controller 7 uses a sleep ON signal simply to reduce a refresh rate (see col. 2, paragraph [0018]-[0020]). Also, White's error correction encoding circuit 3 uses the sleep ON signal to begin encoding the contents of the DRAMs 13 (see paragraph [0020]). Thus White's sleep mode and/or sleep ON signals do not teach or even suggest "turning off a portion of the storage system" as required in claim 1.

Even if White were combined with Trost, the combination still would not teach Appellants' claimed "to conserve power, the storage controller modifies operation of the storage system based on a status of the data transfer, wherein the storage controller modifies operation of the storage system by turning off a portion of the storage system." Instead, the combination would adjust the frequency of a variable rate oscillator based on the fullness of a FIFO buffer as taught in Trost and reduce a DRAM refresh rate when a sleep mode is activated as taught in White. White's sleep mode is only activated based on a predetermined time period elapsing with no user activity (*e.g.*, striking a key or moving a mouse) (see paragraphs [0025] and [0029]). Thus even if White were interpreted to teach turning off the error correction decoding circuit 5 in the sleep mode as suggested by the Examiner, the sleep mode of the combination would still occur after a predetermined time period elapses with no user activity (*e.g.*, striking a key or moving a mouse). Since the proposed modification cannot change the principle of operation of a reference (see MPEP 2143.01), the combination of Trost and White still fails to teach Appellants' claimed "to conserve power, the storage controller modifies operation of the storage system based on a status of the data transfer, wherein the storage controller modifies operation of the storage system by turning off a portion of the storage system." For at least these reasons, claim 1 and its dependent claims are allowable over the cited references.

In addition to the reasons provided with respect to claim 1, claim 6 requires "the storage controller modifies operation of the storage system by turning off the error correction logic of the storage memory interface in the storage system." As previously described, White implements error correction logic including an error

correction encoder 3 and an error correction decoder 5. The error correction encoder 3 performs encodes the contents of White's DRAMs during a sleep mode (see paragraph [0020]). When entering a normal mode, the error correction decoder 5 initiates the detection and correction of errors (see paragraph [0020]). White does not teach or suggest the error correction encoder 3 and error correction decoder 5 are turned off as required by Appellants' claimed "the storage controller modifies operation of the storage system by turning off the error correction logic of the storage memory interface in the storage system." None of the references cited by the Examiner, considered individually or together, teach or suggest the above limitation. For at least these additional reasons, claim 6 is allowable over the cited references.

In addition to the reasons provided with respect to claims 1 and 6, claim 7 requires "an encoder for encoding data to be stored in the storage memory," "a decoder for decoding data retrieved from storage memory" and "wherein the storage controller modifies operation of the storage system by turning off the decoder in the error correction logic of the storage memory interface." As previously described with respect to claim 1, White does not teach or suggest the error correction decoding circuit 5 is turned off in the sleep mode. None of the references cited by the Examiner, considered individually or together, teach or suggest the above limitation. For at least these additional reasons, claim 7 is allowable over the cited references.

In addition to the reasons provided with respect to claims 1, 6 and 7, claim 8 requires "the storage controller turns off the decoder by disconnecting power to the decoder." None of the references cited by the Examiner, considered individually or together, teach or suggest this limitation. For at least this additional reason, claim 8 is allowable over the cited references.

In addition to the reasons provided with respect to claims 1, 6, and 7, claim 9 requires "the storage controller turns off the decoder by disconnecting a clock signal to the decoder." None of the references cited by the Examiner, considered individually or together, teach or suggest this limitation. For at least this additional reason, claim 9 is allowable over the cited references.

Appl. No. 09/998,513
Pre-Appeal Brief dated March 14, 2006
Reply to final Office action of November 16, 2005

Appellants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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